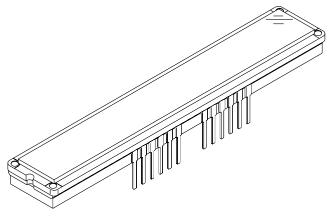
SONY

ILX585K

10680 pixel× 6line CCD Linear Sensor (Color)

24 pin DIP (Plastic)



Description

The ILX585K is reduction type CCD linear sensor developed for color image scanner.This sensor reads A4-size documents at a density of 1200DPI and 2400DPI

Sensor Line Features

2400DPI staggered

Number of effective pixels:
64080 pixels(10680pixels×6)
Pixel size: 4μm×4μm(4μm pitch)
Distance between main line : 48μm(12 lines)
Distance between main line and Sub line: 8μm(2 lines)

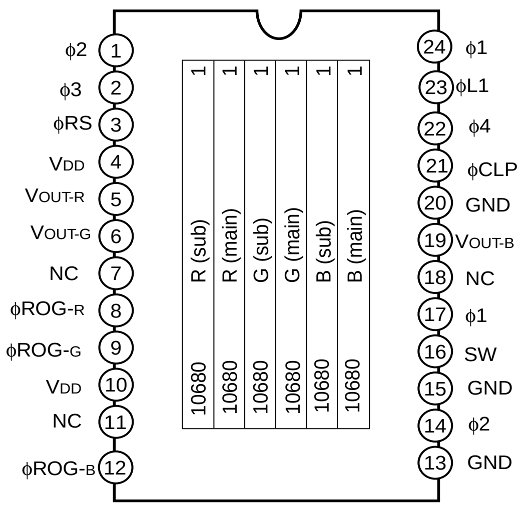
Common Features

Single-sided readout
Ultra low lag
Single 12V power supply
Maximum data rate: 10MHz/Color
Input clock pulse: CMOS 5V drive
Number of output: 3(R,G,B)
Package: 24pin Plastic-DIP(400mil)

Absolute Maximum Ratings

Supply voltage V_{DD} 15 V
Operating temperature −10to+55 ℃

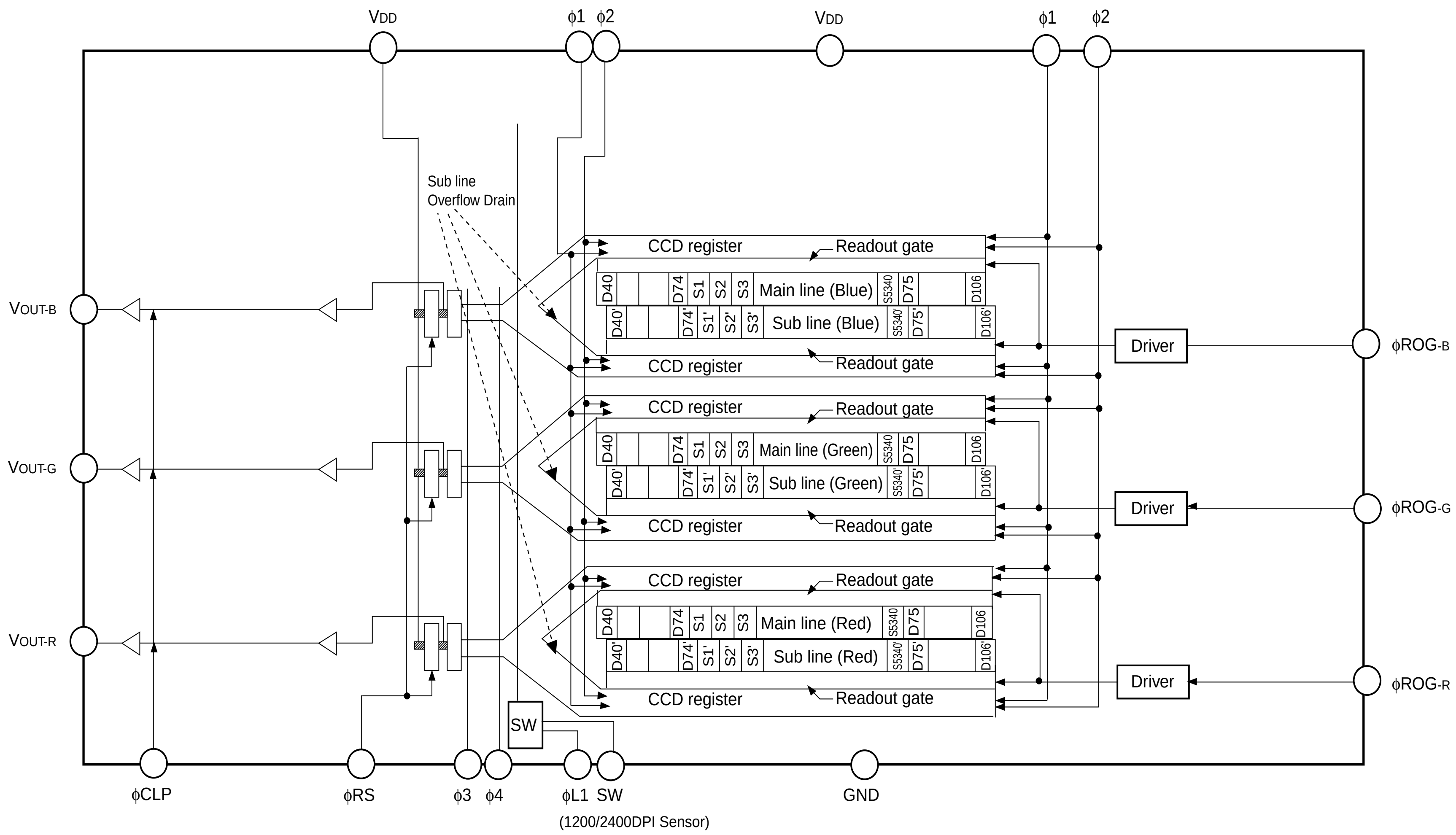
Pin Configuration(Top View)



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits.

02.07.30

Block Diagram



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$\phi 2$	Clock pulse input	13	GND	GND
2	$\phi 3$	Clock pulse input	14	$\phi 2$	Clock pulse input
3	ϕRS	Clock pulse input	15	GND	GND
4	V_{DD}	12V power supply	16	SW	Switch(1200/2400dpi)
5	V_{OUT-R}	Signal output (red)	17	$\phi 1$	Clock pulse input
6	V_{OUT-G}	Signal output (green)	18	NC	NC
7	NC	NC	19	V_{OUT-B}	Signal output (blue)
8	ϕROG_{-R}	Clock pulse input	20	GND	GND
9	ϕROG_{-G}	Clock pulse input	21	ϕCLP	Clock pulse input
10	V_{DD}	12V power supply	22	$\phi 4$	Clock pulse input
11	NC	NC	23	$\phi L1$	Clock pulse input
12	ϕROG_{-B}	Clock pulse input	24	$\phi 1$	Clock pulse input

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of $\phi 1$, $\phi 2$	$C_{\phi 1}$, $C_{\phi 2}$	—	3000	—	pF
Input capacity of ϕRS	$C_{\phi RS}$	—	10	—	pF
Input capacity of ϕROG	$C_{\phi ROG}$	—	10	—	pF
Input capacity of $\phi 3$, $\phi 4$, $\phi L1$	$C_{\phi L1}$, $C_{\phi 3}$, $C_{\phi 4}$	—	20	—	pF

Clock Frequency

2400 DPI Staggered

Item	Symbol	Min.	Typ.	Max.	Unit
ϕ1, ϕ2, ϕL1	$f_{\phi 1}$, $f_{\phi 2}$, $f_{\phi L1}$	—	1	5*1	MHz
ϕ3, ϕ4, ϕRS	$f_{\phi 3}$, $f_{\phi 4}$, $f_{\phi RS}$	—	1	10	MHz

***1 The frequency is 10MHz during the dump mode.**

Input Clock Pulse Voltage Condition

Item		Min.	Typ.	Max.	Unit
ϕ1, ϕ2, ϕRS, ϕROG, ϕL1, ϕ3, ϕ4 pulse voltage	High level	4.75	5.0	5.25	V
	Low level	0	0	0.1	V

SW mode

	SW
HI (5V)	1200 DPI
LO (0V)	2400 DPI

Electrooptical Characteristics (Note 1, 2)

(Ta=25c,VDD=12V, ffRS=1MHz, Input clock=5Vp-p, Light source=3200K, IR cut filter CM500S (t = 1.0mm)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	1.4	2.0	2.6	V/(lx•s)	Note 2
	Green	R_G	1.8	2.6	3.4		
	Blue	R_B	1.4	2.0	2.6		
Sensitivity nonuniformity		PRNU	—	4	20	%	Note 3
Saturation output voltage		V_{SAT}	2.0	2.5	—	V	Note 4
Saturation exposure	Red	SE_R	—	1.25	—	lx•s	Note 5
	Green	SE_G	—	0.96	—		
	Blue	SE_B	—	1.25	—		
Saturation electrons		Nelec	—	30	—	Ke-	at 2.0V
Dark voltage average		V_{DRK}	—	0.1	1.6	mV	Note 6
Dark signal nonuniformity		DSNU	—	0.5	3.2	mV	
Supply current		I_{VDD}	—	30	60	mA	Note 7
Total transfer efficiency		TTE	92	98	—	%	
Output impedance		ZO	—	360	—	Ω	

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Offset level	V_{OS}	—	5.8	—	V	Note 8
Random Noise	$ND\sigma$	—	0.6	—	mV	Note 9

Notes:

1. In accordance with the given electrooptical characteristics, the black level is defined as the average value of D40, D41 to D73.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. PRNU us defubed as indicated below. Ray iincidence conditions are the same as for Note 2.
   Vout=500mV(typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 \ [\%]$$

4. Use below the minimum value of the saturation output voltage.

5. Saturation exposure is defined as follows.

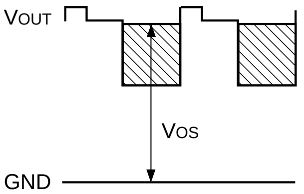
   $$SE = \frac{V_{SAT}}{R}$$

   Where R indicates R_R, R_G, R_B and SE indicates SE_R, SE_G, SE_B.

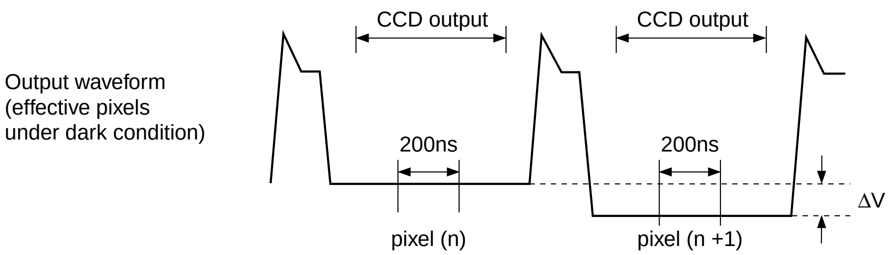
6. Optical signal accumulated time τint stands at 4ms.

7. Supply current means the total current of this device.

8. Vos is defined as indicated bellow.
   V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, and V_{OUT-B}.



9. Random noise is defined on the output waveform with the external clamp and is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e.dark conditions) calculated by the following procedure.



a) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
b) Each of the output level at video output periods is averaged over 200ns period to get V (n) and V (n + 1).
c) V (n + 1) is subtracted from V (n) to get ƒ¢V.

   ƒ¢V = Vn •|V (n + 1)

d) The standard deviation of ƒ¢V is calculated after procedure b) and c) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta Vi| \bullet |\overline{\Delta V})^2}$$

e) Procedure b), c) and d) are repeated 10 times to get sigma value.

f) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{i=1}^{10} \sigma j$$

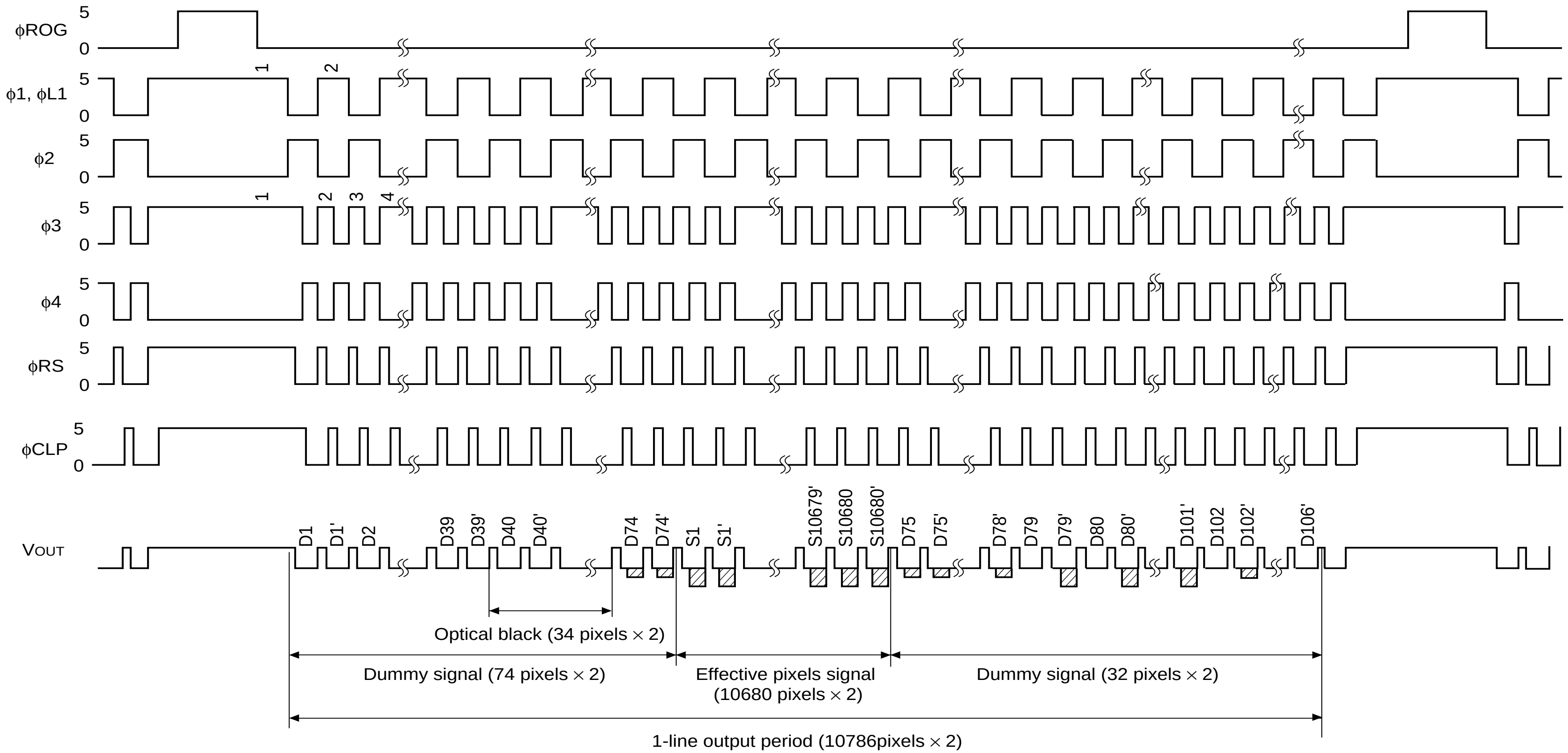
g) $\overline{\sigma}$ value calculated using the above procedure is observed √2 times larger than that measured relative to the ground level. So we specify random noise as follows.

$$ND\sigma = \frac{1}{\sqrt{2}} \overline{\sigma}$$

Clock Timing Chart 1   2400 DPI Staggered(pixel clamp mode)

SW mode

SW	L

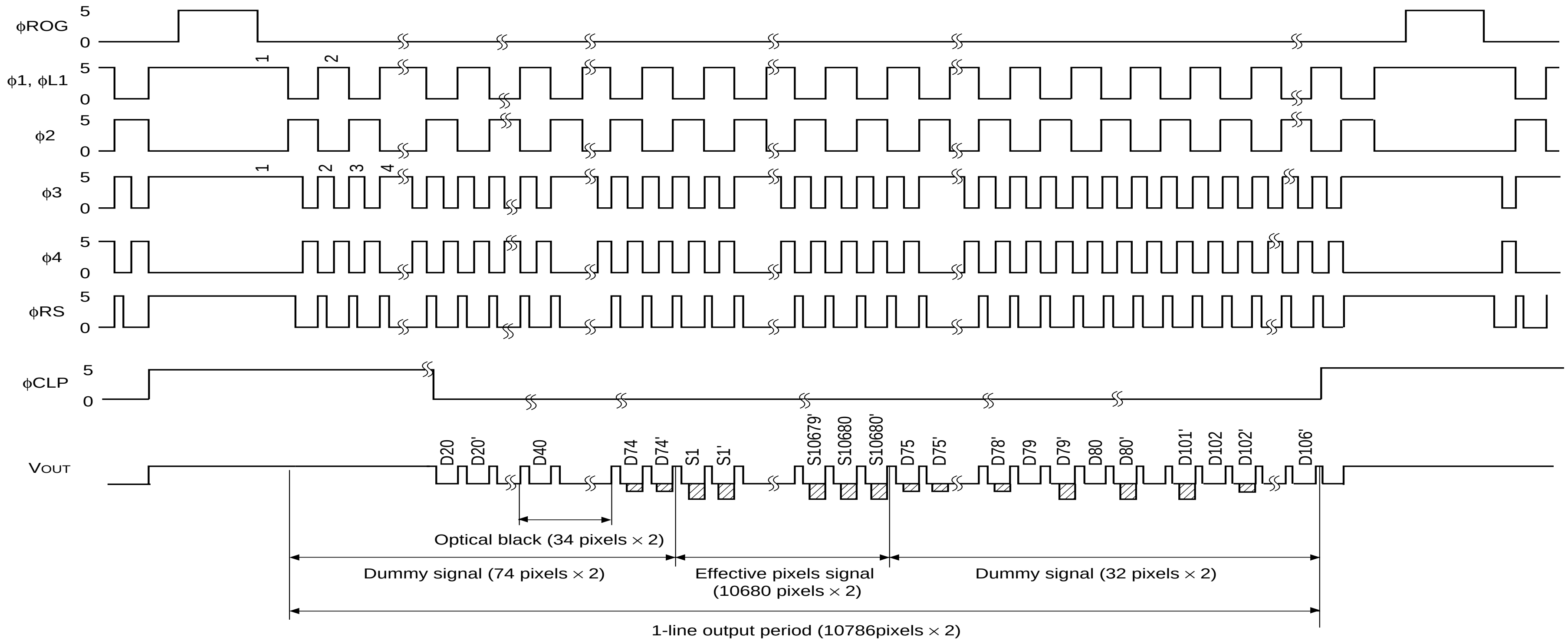


Note) The transfer pulses (φ1, φ2) must have more than 10786 cycles.
The transfer pulses (φ3, φ4) must have more than 21572 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 2   2400 DPI Staggered(line clamp mode)

SW mode

SW	L

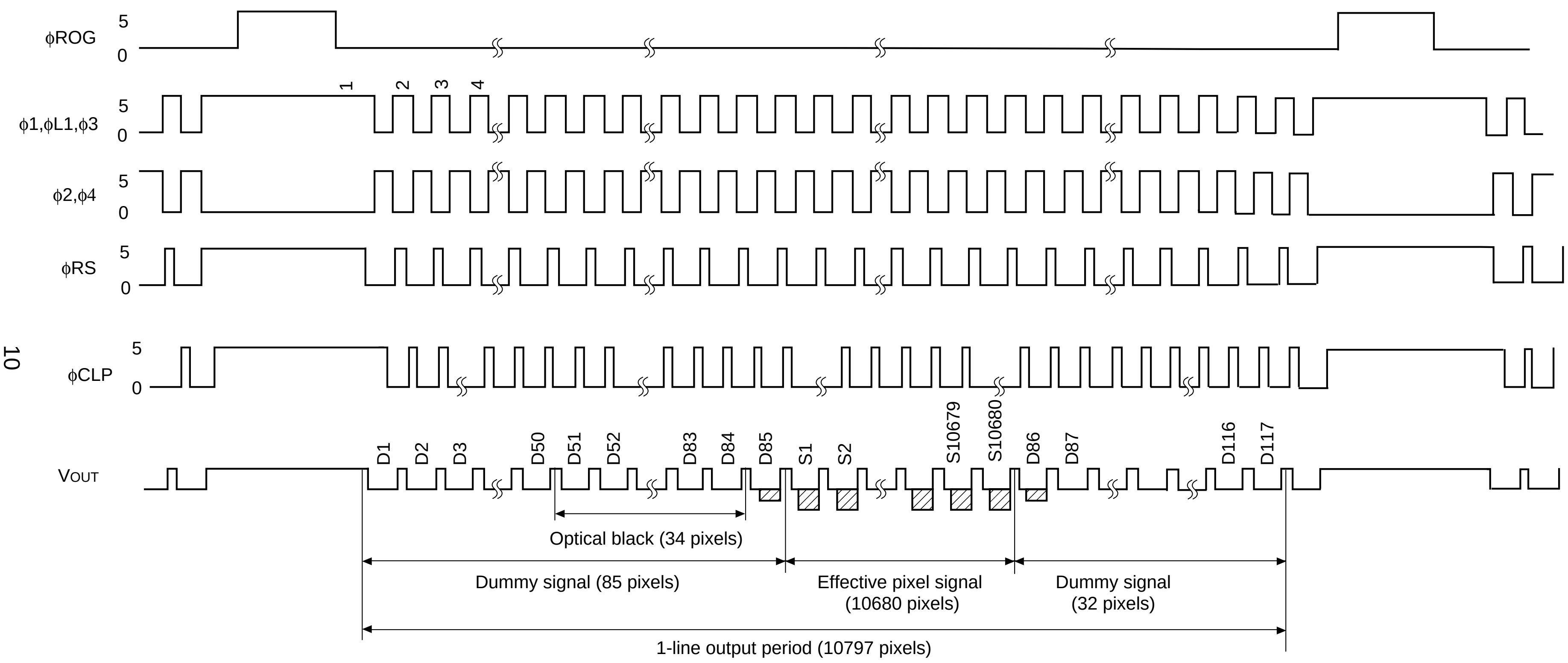


Note) The transfer pulses (φ1, φ2) must have more than 10786 cycles.
The transfer pulses (φ3, φ4) must have more than 21572 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 3   1200 DPI Linear(pixel clamp mode)

SW mode

SW	H

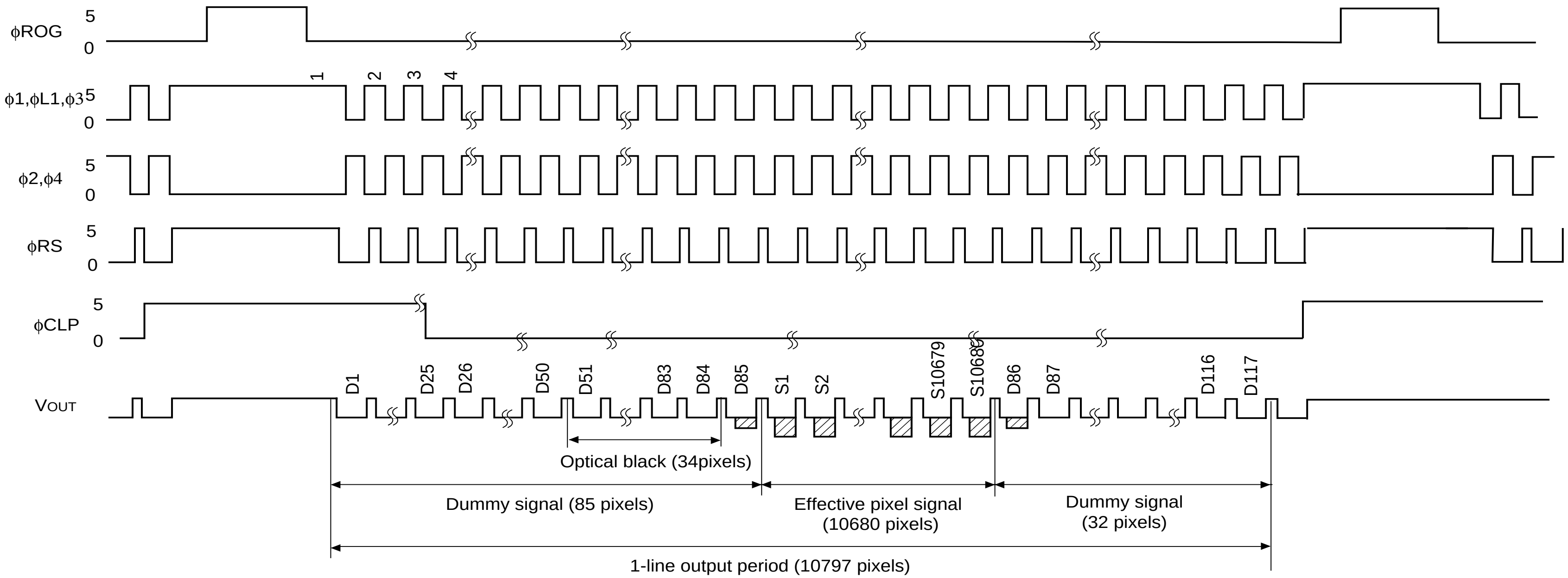


Note) The transfer pulses (φ1, φ2) must have more than 10797 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 4 1200 DPI Linear(line clamp mode)

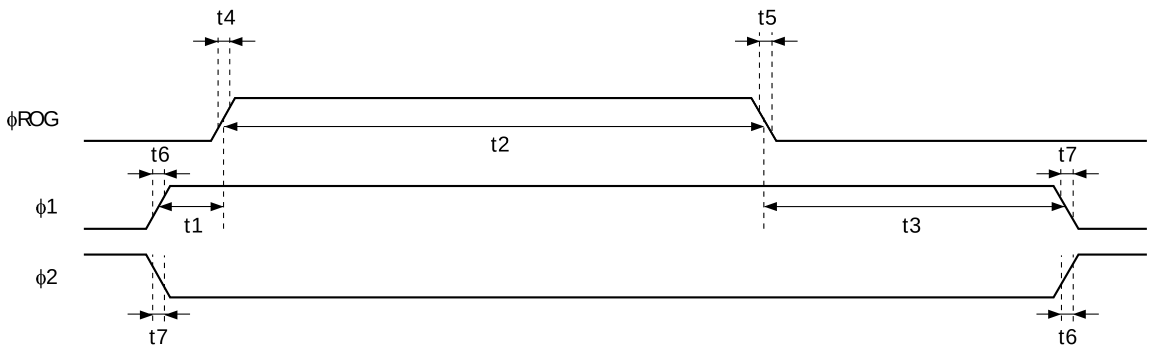
SW mode

SW	H

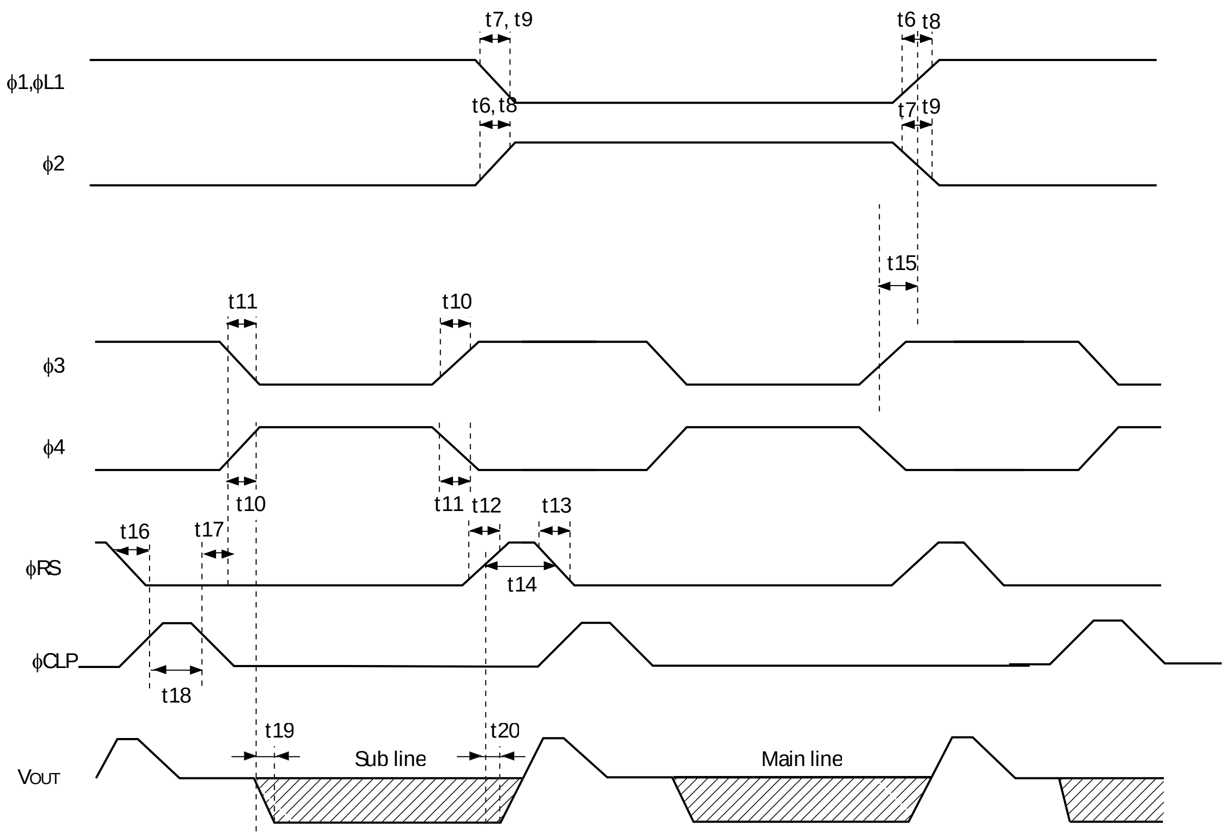


Note) The transfer pulses (φ1, φ2) must have more than 10797 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

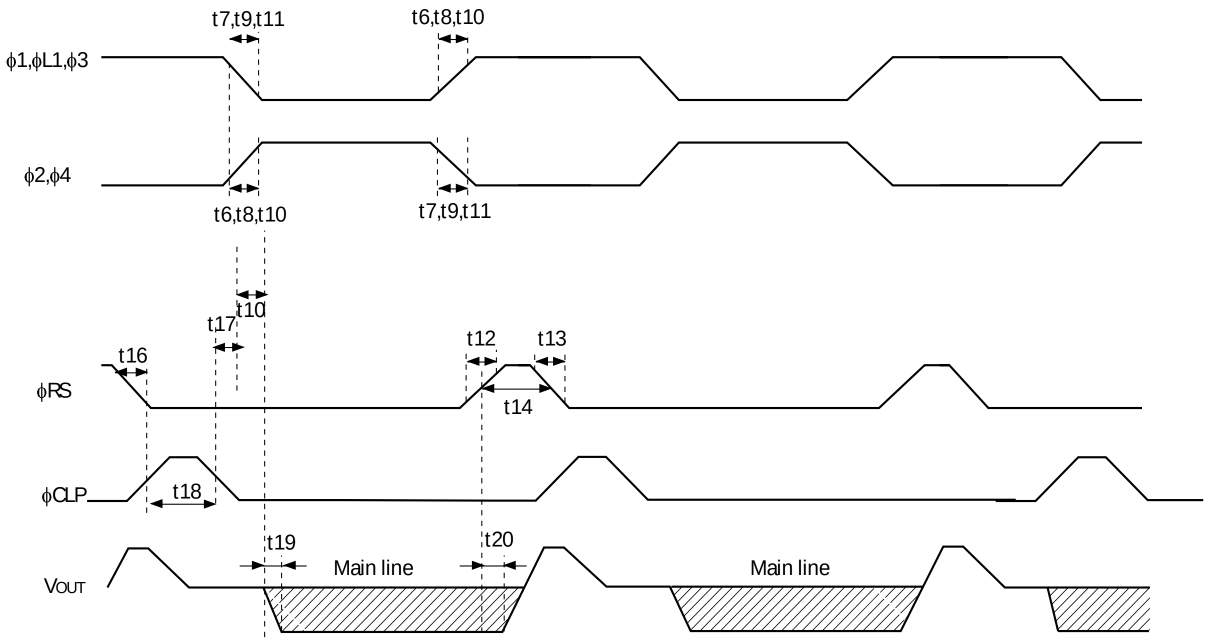
Clock Timing Chart5 2400 DPI Staggered



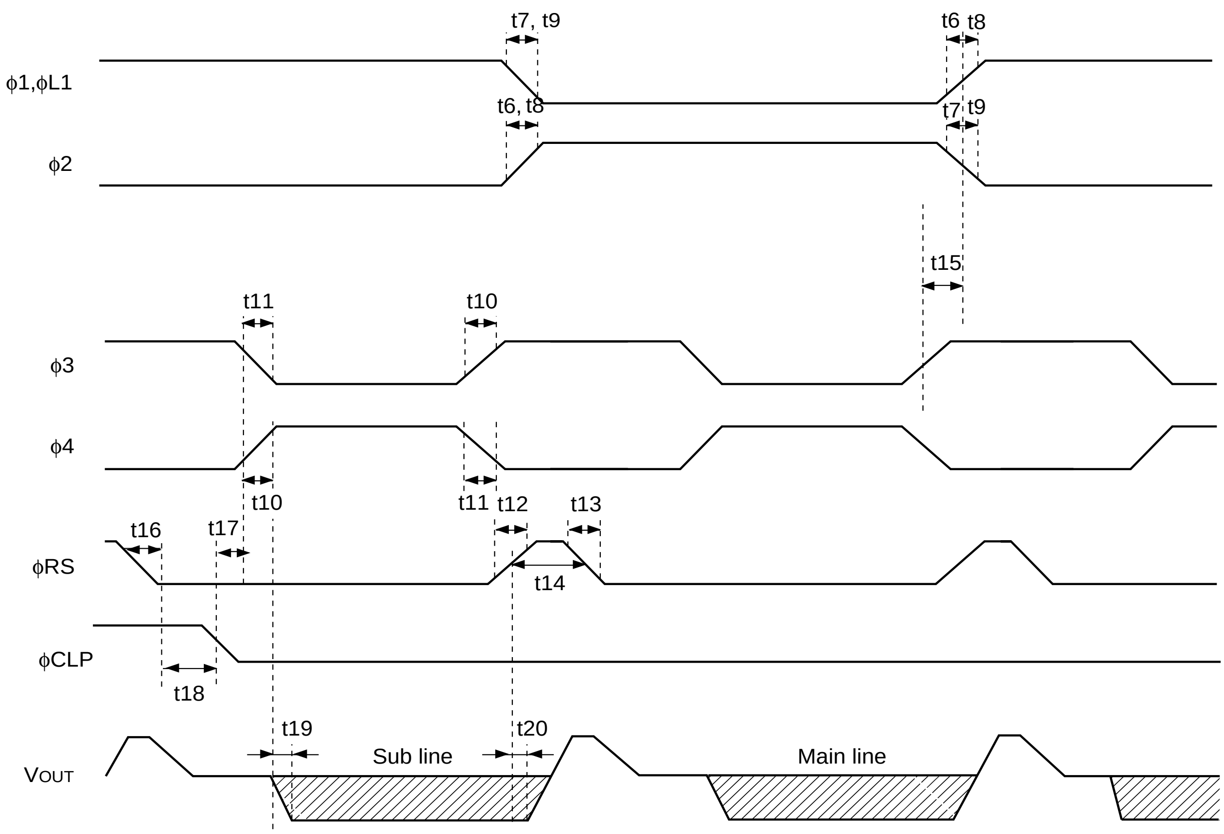
ClockTiming Chart 6
(2400 DPI pixel clamp mode)



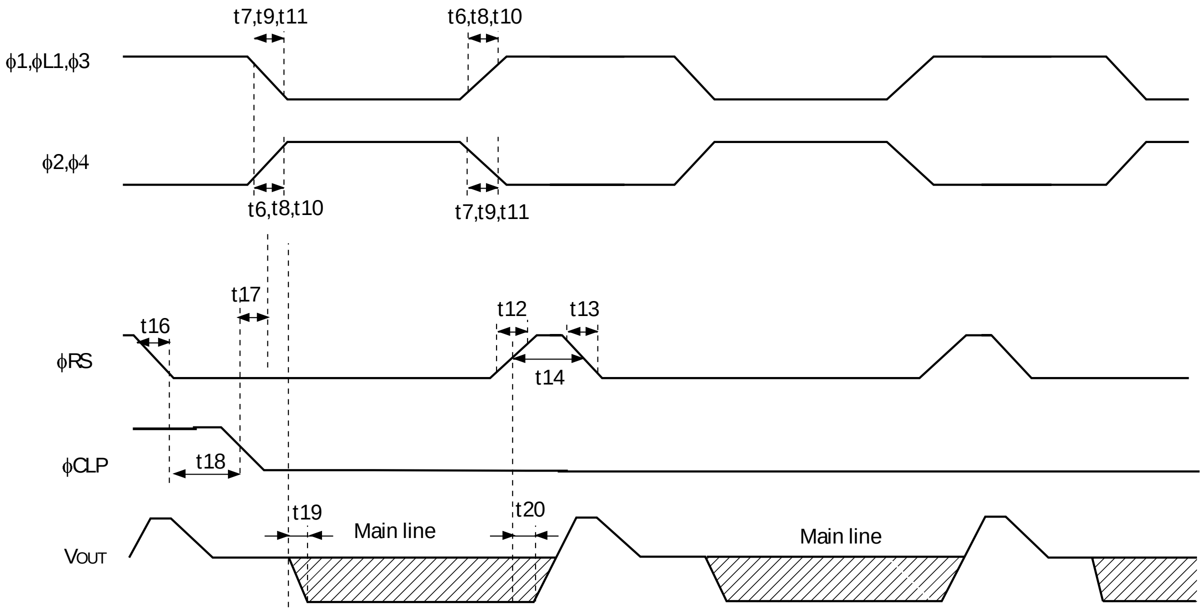
ClockTiming Chart 7
(1200 DPI pixel clamp mode)



ClockTiming Chart 8
(2400 DPI line clamp mode)



ClockTiming Chart 9
(1200 DPI line clamp mode)

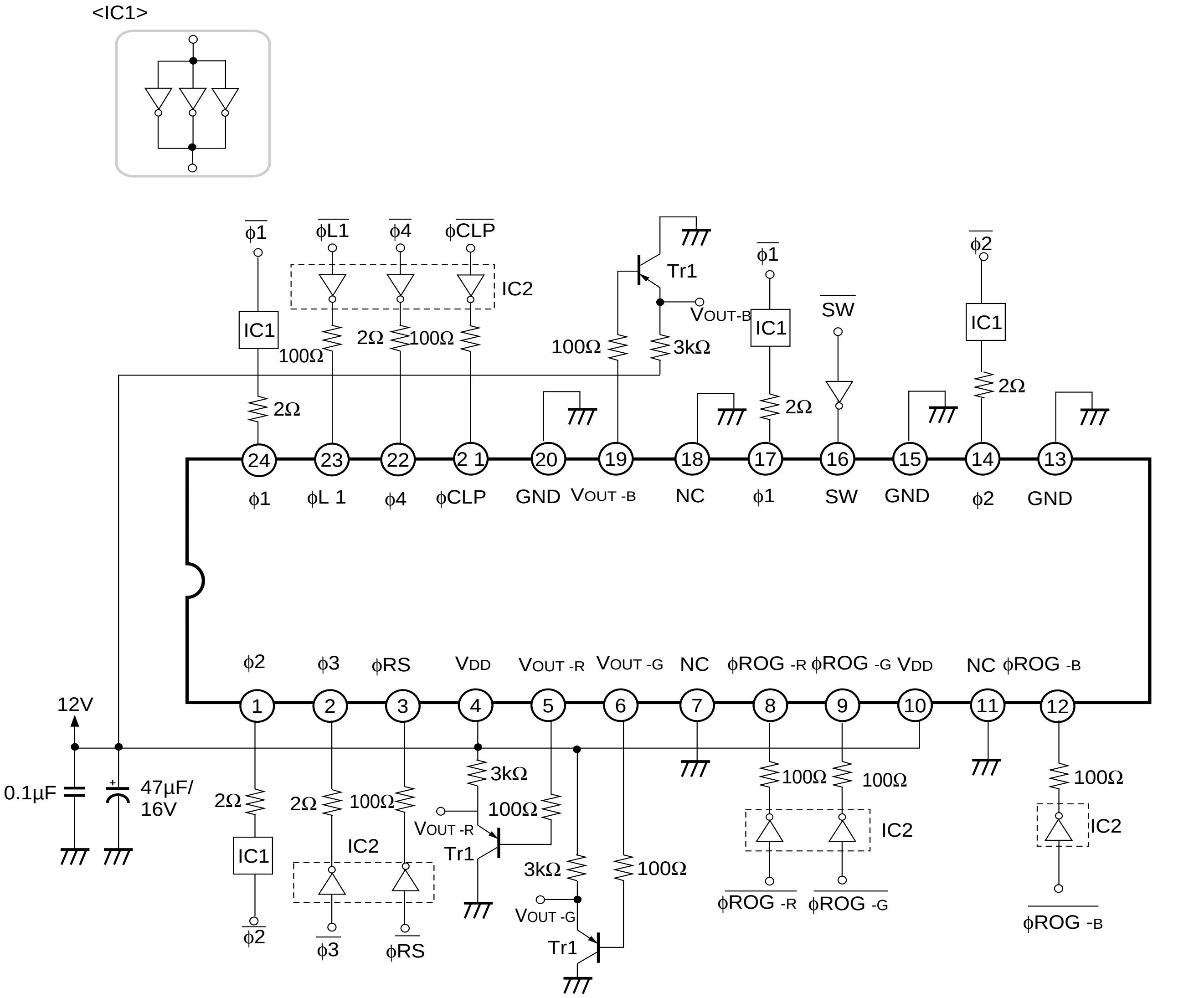


Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φ1 pulse timing	t1	50	100	—	ns
φROG pulse high level period	t2	5	10	—	μs
φROG, φ1 pulse timing	t3	3	5	—	μs
φROG pulse rise time	t4	0	5	10	ns
φROG pulse fall time	t5	0	5	10	ns
φ1 pulse rise time/φ2 pulse fall time	t6	0	50	80	ns
φ1 pulse fall time/φ2 pulse rise time	t7	0	50	80	ns
φL1 pulse rise time/φ2 pulse fall time	t8	0	10	30	ns
φL1 pulse fall time/φ2 pulse rise time	t9	0	10	30	ns
φ3 pulse rise time/φ4 pulse fall time	t10	0	10	30	ns
φ3 pulse fall time/φ4 pulse rise time	t11	0	10	30	ns
φRS pulse rise time	t12	0	10	30	ns
φRS pulse fall time	t13	0	10	30	ns
φRS pulse high level period	t14	30	100*1	—	ns
φL1,φ2-φ3 pulse timing	t15	0	10	—	ns
φRS,φCLP pulse timing	t16	0	250*1	—	ns
φCLP,φL1,φ3 pulse timing	t17	60	250*1	—	ns
φCLP pulse high level period	t18	20	100	—	ns
Signal output delay time	t19	—	40	—	ns
	t20	—	20	—	ns

*1 These timing is the recommended condition under $f_{\phi RS}$ = 1MHz.

Application Circuit*



IC1: 74AC04 × 3pcs
IC2: 74HC04
Tr1: 2SA1175

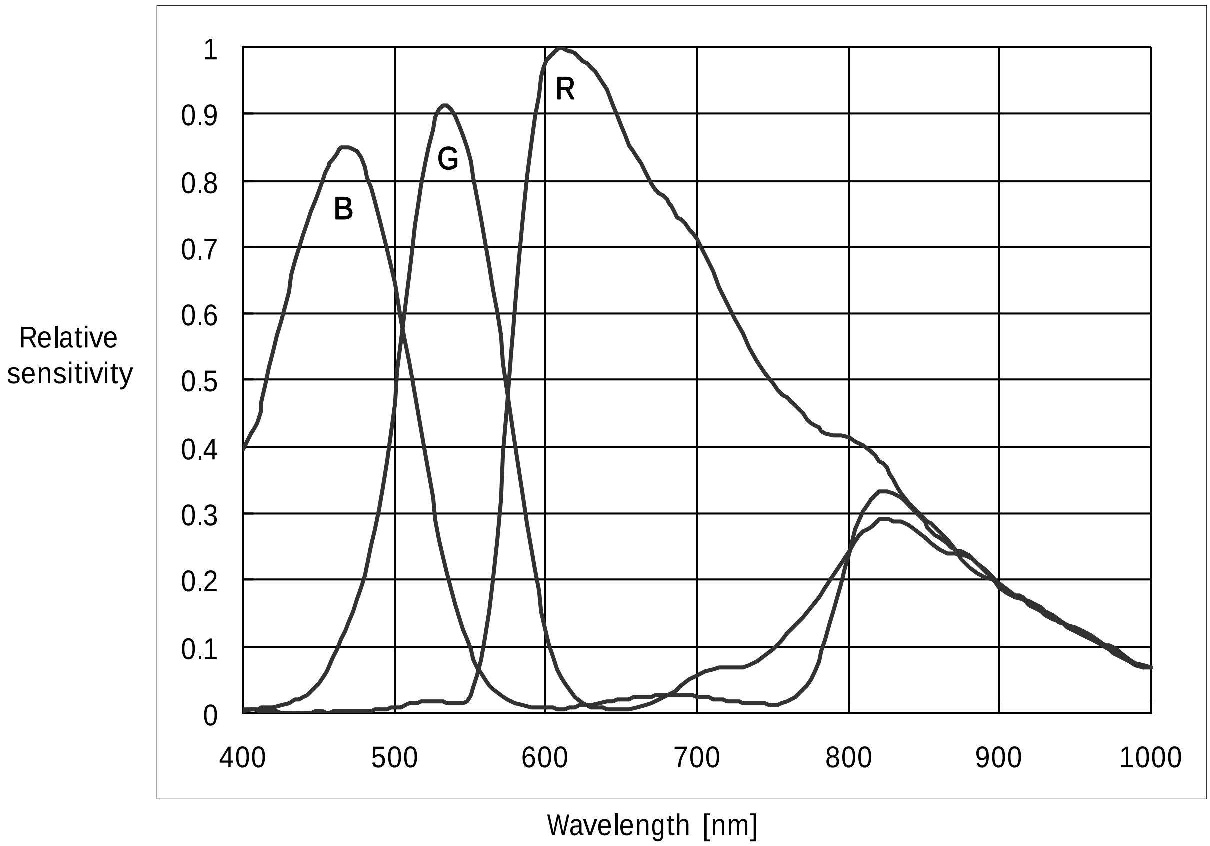
* Data rate fφRS = 1MHz

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

<2400DPI>

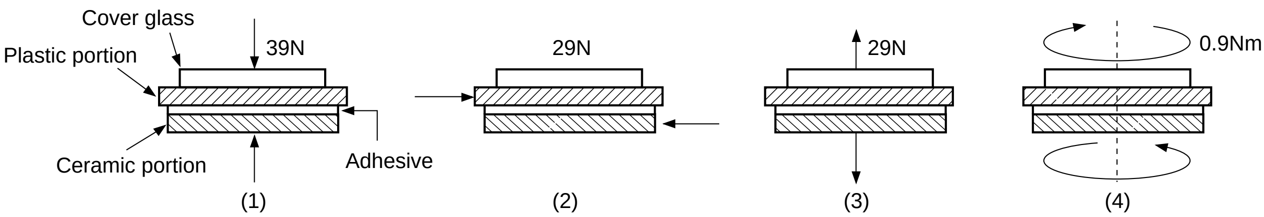
Spectral sensitivity characteristics (Standard characteristics)



Notes of Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Packages
   The following points should be observed when handling and installing packages.
   a) Remain within the following limits when applying static load to the package:
      (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
      (2) Shearing strength: 29N/surface
      (3) Tensile strength: 29N/surface
      (4) Torsional strength: 0.9Nm



   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
   c) Be aware that any of the following can cause the package to crack or dust to be generated.
      (1) Applying repetitive bending stress to the external leads.
      (2) Applying heat to the external leads for an extended period of time with soldering iron.
      (3) Rapid cooling or heating.
      (4) Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
      (5) Applying the metal a crash or a rub against the plastic portion.
      Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.
   d) The notch of the plastic portion is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch or ceramic may overlap with the notch of the plastic portion.
3) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

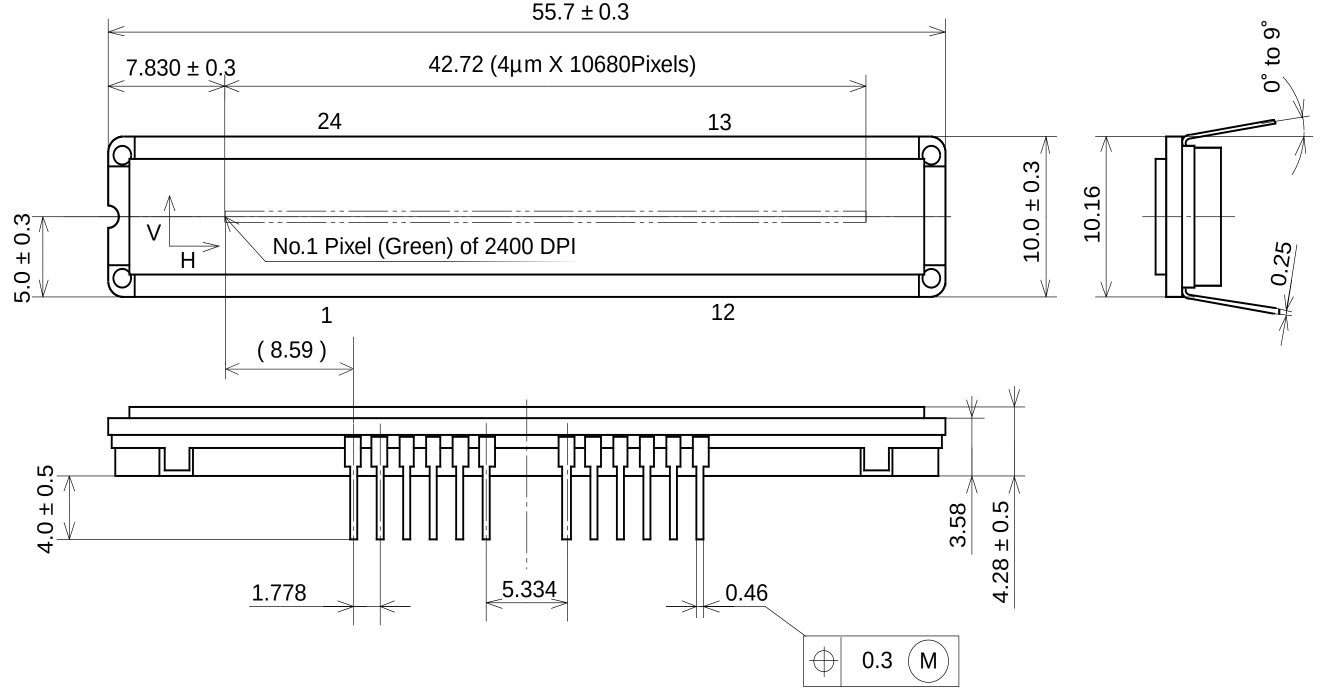
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline

Unit: mm

24 pin DIP (400mil)



1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic, Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.43g
DRAWING NUMBER	LS-B41(E)